FORM PTO-1390 REV. 5-93	US DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEYS DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		P00,1889
		U.S. APPLICATION NO. (if known, see 37 CFR 1.5) 09/701593
INTERNATIONAL APPLICATION NO. PCT/DE99/01555	INTERNATIONAL FILING DATE 25 MAY 1999	PRIORITY DATE CLAIMED 29 MAY 1998

TITLE OF INVENTION
APPARATUS AND METHOD FOR THE SYNCHRONIZATION OF AN ASYNCHRONOUS SIGNAL IN SYNTHESIS AND SIMULATION OF A CLOCKED CIRCUIT

APPLICANT(S) FOR DO/EO/US **MARTIN MÄNZ, ET AL.**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay.
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of International Application as filed (35 U.S.C. 371(c)(2)) - drawings attached.
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2) - drawings attached.

7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98; **(PTO 1449, Prior Art, Search Report)**.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
    (SEE ATTACHED ENVELOPE)

13. ☒ Amendment "A" Prior to Action.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☒ A change of address letter attached to the Declaration.

16. ☒ Other items or information:
    a. ☒ Appointment of Associate Power of Attorney

    b. ☒ EXPRESS MAIL #EL655299356US dated November 29, 2000.

529 Rec'd PCT/PTC 29 NOV 2000

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/701593	PCT/DE99/01555	P00,1889

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5): Search Report has been prepared by the EPO or JPO $860.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) . . $690.00		
No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO (37 C.F.R. 1.445(a)(2) $710.00		
Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2) paid to USPTO $1000.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) . . . . . $ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$	

Claims	Number Filed		Number Extra	Rate		
Total Claims	20	- 20 =	0	X $ 18.00	$	
Independent Claims	02	- 3 =	0	X $ 80.00	$	
Multiple Dependent Claims				$270.00 +	$	
				TOTAL OF ABOVE CALCULATIONS =	$ 860.00	
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 C.F.R. 1.9, 1.27, 1.28)					$	
				SUBTOTAL =	$ 860.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				+	$	
				TOTAL NATIONAL FEE =	$ 860.00	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property				+		
				TOTAL FEES ENCLOSED =	$ 860.00	
				Amount to be refunded	$	
				charged	$	

a. ☒ A check in the amount of $ 860.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **501519**. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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BOX PCT
IN THE UNITED STATES DESIGNATED/ELECTED OFFICE
OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY--CHAPTER II

APPLICANT(S):	MARTIN MÄNZ, ET AL.
ATTORNEY DOCKET NO.:	P00,1889
INTERNATIONAL APPLICATION NO:	PCT/DE99/01555
INTERNATIONAL FILING DATE:	25 MAY 1999
INVENTION:	APPARATUS AND METHOD FOR THE SYNCHRONIZATION OF AN ASYNCHRONOUS SIGNAL IN SYNTHESIS AND SIMULATION OF A CLOCKED CIRCUIT

Assistant Commissioner for Patents,
Washington D.C. 20231

AMENDMENT A PRIOR TO ACTION

Sir:

Applicants herewith amend the above-referenced PCT application, and request entry of the Amendment prior to examination on the United States Examination Phase.

IN THE SPECIFICATION:

On page 1:

replace lines 1-3, with

--SPECIFICATION

TITLE

APPARATUS AND METHOD FOR THE SYNCHRONIZATION OF AN ASYNCHRONOUS SIGNAL IN SYNTHESIS AND SIMULATION OF A CLOCKED CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention--;

above line 9, insert

--Description of the Related Art--;

in line 10, replace "circuit" with --circuits--;

in line 11, cancel "the", cancel "their", and replace "in advance" with –prior to manufacture--;

replace line 12 with –by simulation.--;

in line 13, cancel "thereby", and after "described", insert –for simulation--;

in line 14, cancel ", for example,";

in line 18, cancel "on the contrary,";

in line 20, replace "for presenting" with –of--;

in line 22, cancel ", respectively,";

in line 23, replace "Given" with –For--;

in lines 23-24, cancel ", respectively,";

in lines 24-25, replace "already be" with –have been--;

in line 25, replace "Let such" with –Such--, and after "status", insert –may--; and

in line 26, replace "whereby, however," with –but--.

On page 2:

in line 1, replace "Figure a" with –Figure 1--;

in line 5, cancel ", respectively,";

in line 6, before "flip-flop", insert –a--;

in line 7, cancel "thereby";

in line 14, replace "Compared thereto" with –In comparison--;

in line 20, replace "whereby" with –where--;

in line 23, replace "wherein" with –in which--;

in line 26, replace "given" with –for a--; and

in line 27, after "i.e.", insert –,–, and cancel ", respectively,".

On page 3:

in line 1, replace "referred to in general" with –generally referred to--;

in lines 3-4, cancel ", or respectively";

in line 6, replace ", and signals or, respectively," with –. Signals or--;

in line 7, after "this", insert –affected--;

in line 8, before "abort", insert –e.g., an–;

in line 13, replace "as a result whereof the problems derives" with –resulting in the problem–;

in line 14, replace "output" with –outputs–;

in line 15, replace "A_ASYNC" with –S_ASYNC–;

in line 16, replace "can thus necessarily" with –will–;

in line 17, replace "Given" with –FOR–;

in line 18, replace "can thus" with –thus can–;

in line 23, replace "S_ASYNCH" with –S_ASYNC–;

in line 24, replace "comprised in undertaking" with –to perform–;

in line 25, cancel ", respectively,";

in line 26, replace "form" with –from–; and

in line 27, after "error", insert –,–.

On page 4:

above line 1, insert

–SUMMARY OF THE INVENTION–;

in line 3, replace "whereby" with –by which–;

replace lines 5-7 with

– This object is achieved by a method for the synchronization of an asynchronous signal in synthesis and simulation of a clocked circuit, comprising the steps of: a) describing the clocked circuit with a first code in a hardware description language; b) marking asynchronous signals of the clocked circuit in the first code; c) implementing a synthesis of the first code for producing a second code in a network list format, and inserting a synchronization module at every marking; d) implementing a logic/timing simulation at the second code for testing time behavior of signals in the clocked circuit, and selectively deactivating the test of the time behavior for each inserted synchronization module by adaptation in a simulation model of the appertaining synchronization module; and e) displaying occurring, undefined signal-time behavior in the clocked circuit.

This object is also achieved by an apparatus for detecting undefined signal-time behavior in a clocked circuit comprising: a) an input for a first code describing a clocked circuit in a hardware description language; b) a first memory for storing the

first code; c) a marking mechanism for marking asynchronous signals in the first code; d) a synthesis mechanism that produces a second code in a network list format from the first code and stores this in a second memory, a synchronization module being inserted at every marking; e) a timing simulator that implements a timing simulation at the second code for testing time behavior of signals of the clocked circuit, the test of the time behavior being selectively deactivated for each inserted synchronization module by adaptation in a simulation model of an appertaining synchronization module; f) a display for displaying occurring, undefined signal-time behavior; and g) a bus structure that connects the input, the first memory, the second memory, the marking mechanism, the display, the synthesis mechanism, and the timing simulator to one another. --

in line 9, after "language", insert --,--;

in line 10, replace "ensues" with –takes place--, and replace "whereby" with –in which--;

in line 12, replace "whereby" with –in which--;

in line 18, cancel "thereby";

in line 19, after "as", insert –a--;

in line 20, replace "this being composed of" with –which comprises--, and replace "whereby" with –in which--;

above line 23, insert

--BRIEF DESCRIPTION OF THE DRAWINGS --;

in line 24, cancel "Shown are:";

in line 25, before "a circuit", insert –is--;

in line 27, replace "an illustration of" with –is a circuit diagram illustrating--; and

in line 28, replace ", whereby" with –in which--.

On page 5:

in line 1, replace "an illustration of" with –is a circuit diagram illustrating--;

in line 2, replace "whereby" with –in which--;

in line 3, before "a block", insert –is--;

in line 4, before "a block", insert –is--;

in line 6, replace "an illustration of" with –is a diagram illustrating--;

in line 8, replace "an illustration of" with –is a diagram illustrating--;

in line 10, before "a block", insert –is–;

in line 11, replace "an illustration of" with –is a timing diagram illustrating–;

in line 13, replace "an illustration of" with –is a timing diagram illustrating–;

above line 15, insert

--DESCRIPTION OF THE PREFERRED EMBODIMENTS--;

in line 16, cancel "thereby";

in line 20, cancel "thereby" and replace "whereby, however," with –but–; and

in line 22, replace "comprising [sic]" with –comprises–, and after "FF1", insert --,--.

On page 6:

in line 13, replace "undertaken" with –performed–;

replace line 14 with –As noted above, however, a–;

in line 20, cancel "As";

replace line 21 with –Setup time–;

in line 22, cancel "thereby";

in line 23, cancel ", respectively,"

in line 24, cancel ", respectively,"

in line 25, replace "and" with –preventing testing of–;

in line 26, cancel "can no longer be tested"; and

in line 28, cancel ", respectively, the inventive".

On page 7:

in line 2, replace ", whereby" with –in which–;

in line 3, replace "..." with --, etc.–;

in lines 3-4, replace "that has arisen" with –created–;

in line 6, replace "ensues" with –takes place", and replace "whereby" with –in which–;

in line 7, cancel ", or respectively,";

in line 10, cancel ", for example,";

in line 12, replace "shows an illustration of" with –illustrates--; and

in line 26, replace "over and above this" with –additionally--.

On page 8:

replace lines 7-9 with –interpreted as an unknown status, creating an unknown status for all signals that depend on output signal S3.--;

in line 11, cancel "=";

in line 17, replace "wherein" with –in which--;

in line 18, cancel ", respectively,";

in line 20, replace "ensue" with –take place--;

in line 21, cancel ", namely,";

in line 24, after "as", insert –a--;

in line 25, after "as", insert –a--; and

in line 28, replace ", whereby the time t_{logic}" with –in which the time t_{LOGIK}--.

On page 9:

in line 2, replace "fli-flop" with –flip-flop--;

in line 5, cancel "supplied [sic]";

in line 10, replace "as a result whereof" with –resulting in--;

in line 11, cancel "derives";

in line 16, replace ", wherewith [sic]" with –in which–;

in line 21, cancel "thereby" and replace ", whereby" with --. In this module,--;

in line 23, cancel "thereof";

in line 25, replace "was" with –has been--;

replace line 27 with –set with the trailing edge, or a system combining both leading and trailing edge flip-flops may be used.—

in line 28, cancel "employed."; and

in line 29, replace "wherein" with –in which--.

On page 10:

in line 8, after "IC", insert --,--;

in line 11, replace "whereby" with –by which--;

in line 12, cancel ", respectively,";

in line 13, replace ", whereby" with –in which--;

in line 16, replace ", whereby" with –in which--;

in line 19, after "i.e.", insert --,--;

in line 20, after "as", insert –the--;

in line 23, cancel ", respectively,";

in line 25, replace "and" with –which permits--; and

in lines 25-26, cancel "is possible".

On page 11:

in line 2, replace "means 1, of" with –1, --;

in line 3, cancel "means";

in line 4, cancel "of", and after "i.e.", insert --,--;

in line 5, replace "means" with –mechanism--;

in line 8, replace "means" with –mechanism--;

in line 10, replace "as a result whereof" with –resulting in--;

in line 11, replace "As was already set forth above, the" with –The--;

in line 14, replace "whereby it" with –which--;

in line 16, replace "means 5, whereby" with –5, and--;

in line 17, replace "means" with –elements--;

in line 18, replace ", whereby the" with --. The--;

in line 19, replace "means" with –mechanism--;

in line 20, after "central", insert –processing--; and

below line 20, insert

-- The above-described method and apparatus are illustrative of the principles of the present invention. Numerous modifications and adaptations thereof will be readily apparent to those skilled in this art without departing from the spirit and scope of the present invention.--.

IN THE CLAIMS:

On substitute page 12:

replace line 1 with --WHAT IS CLAIMED IS:--;

Please amend the following claims 1-18.

1. (Amended) A method [Method] for the synchronization of an asynchronous signal in synthesis and simulation of a clocked circuit, comprising the steps of:

a) describing said [the] clocked circuit with a first code [(VHDL)] in a hardware description language;

b) marking asynchronous signals of said [the] clocked circuit in said [the] first code [(VHDL)];

c) synthesizing [implementing a synthesis of] said [the] first code [(VHDL)] for producing a second code in a network list format, and inserting [whereby] a synchronization module [(IFF) is inserted] at every said marking;

d) implementing a logic or [/] timing simulation at said [the] second code for testing [the] time behavior of [the] signals in said [the] clocked circuit, and selectively deactivating said [whereby the] test of said [the] time behavior [is selectively deactivated] for each inserted synchronization module [(IFF)] by adaptation in a [the] simulation model of the appertaining synchronization module; and

e) displaying occurring, undefined signal-time behavior in said [the] clocked circuit.

2. (Amended) The method [Method] according to [patent] claim 1, comprising the further step of:

providing [implementing] a logic simulation at said [the] first code [(VHDL)] for testing a [the] logic function of said [the] clocked circuit.

3. (Amended) The method [Method] according to [patent] claim 1 [or 2], wherein said [whereby the] first code represents a hardware description language and said [the] second code represents a network list.

4. (Amended) The method [Method] according to [patent] claim 3, wherein said [whereby the] hardware description language is [as] a VHDL code.

5. (Amended) The method [Method] according to claim 1, wherein said step of inserting said [one of the claims 1 through 4, whereby the insertion of the] synchronization module implemented in the synthesis of said [the] first code corresponds to inserting [the insertion of] an imaginary flip-flop [(IFF)].

6. (Amended) The method [Method] according to patent claim 5, wherein said [whereby the] imaginary flip-flop comprises [(IFF) is composed of] a first and second flip-flop [(FF2, FF3)] that are clocked with the same clock.

7. (Amended) The method [Method] according to patent claim 5, wherein said [whereby the] imaginary flip-flop comprises [(IFF) is composed of] a first and a second flip-flop [(FF2, FF3)] that are clocked with clocks [(CLK, $\overline{CLK}$)] inverted relative to one another.

8. (Amended) The method [Method] according to claim 6, further comprising the step of selectively deactivating a [one of the patent claims 6 or 7, whereby the] test of [the] signal-time behavior upon said implementation of said [the] timing simulation [is selectively deactivated] only for said [the] first flip-flop [(FF2)].

9. (Amended) The method [Method] according to claim 1, further comprising the step of displaying [one of the patent claims 1 through 8, whereby] a circuit element causing an undefined signal-time behavior [is displayed] when said [the] undefined signal-time behavior is displayed.

10. (Amended) An apparatus [Apparatus] for detecting undefined signal-time behavior in a clocked circuit comprising:

a) an input [means (1)] for [the input of] a first code [(VHDL)] describing a clocked circuit in a hardware description language;

b) a first memory [means (2)] for storing said [the] first code [(VHDL)];

c) a marking mechanism [means (4)] for marking asynchronous signals [(S_ASYNC)] in said [the] first code;

d) a synthesis mechanism [means (6)] that produces a second code in a network list format from said [the] first code [(VHDL)] and stores this in a second memory, [means (3), whereby] a synchronization module [(IFF) is] being inserted at every marking;

e) a timing simulator [(7)] that implements a timing simulation at said [the] second code for testing [the] time behavior of [the] signals of said [the] clocked circuit, [whereby] the test of the time behavior being [is] selectively deactivated for each inserted synchronization module [(IFF)] by adaptation in a [the] simulation model of an [the] appertaining synchronization module;

f) a display [means (5)] for displaying occurring, undefined signal-time behavior; and

g) a bus structure that connects said input, said first memory, said second memory, said marking mechanism, said display, said synthesis mechanism, and said timing simulator [the means (1-7)] to one another.

11. (Amended) The apparatus [Apparatus] according to [patent] claim 10, further comprising [with] a logic simulator [(8)] that implements a logic simulation based on [the basis of the] said first code [(VHDL)] for testing [the] logic behavior of said [the] clocked circuit.

12. (Amended) The apparatus [Apparatus] according to claim 10, wherein said [one of the patent claims 10 or 11, whereby the] first code [codes] represents a hardware description language and said [the] second code represents a network list.

13. (Amended) The apparatus [Apparatus] according to patent claim 12, wherein said [whereby the] hardware description language is a VHDL code.

14. (Amended) The apparatus [Apparatus] according to claim 10, wherein said [one of the patent claims 10 through 13, whereby the] synchronization module corresponds to an imaginary flip-flop [(IFF)].

15. (Amended) The apparatus [Apparatus] according to [patent] claim 14, wherein said [whereby the] imaginary flip-flop comprises [(IFF) is composed of] a first and second flip-flop [(FF2, FF3)] that are clocked with a same clock signal [(CLK)].

16. (Amended) The apparatus [Apparatus]according to [patent] claim 14, wherein said [whereby the] imaginary flip-flop [(IFF) is composed of] comprises a first and a second flip-flop [(FF2, FF3)] that are clocked with clock signals (CLK, $\overline{CLK}$) inverted relative to one another.

17. (Amended) The apparatus [Apparatus] according to claim 15, wherein said [one of the patent claims 15 or 16, whereby the] timing simulator [(7) does not consider the] operates independently of time behavior for said [the] first flip-flop [(FF2)] in the implementation of said [the] timing simulation.

18. (Amended) The apparatus [Apparatus] according to claim 10, wherein said [one of the patent claims 1 through 17, whereby the] display [means (5)] also displays a circuit element causing [the] undefined signal-time behavior.

Please add the following claims 19-20.

19 The method according to claim 7, further comprising the step of selectively deactivating a test of signal-time behavior upon said implementation of said timing simulation only for said first flip-flop.

20. The apparatus according to claim 16, wherein said timing simulator operates independently of time behavior for said first flip-flop in the implementation of said timing simulation.

IN THE ABSTRACT:

On page 15:

cancel lines 2-3;

in line 5, replace ", whereby" with --in which--;

in line 8, replace ", whereby" with --in which--;

in line 11, replace ", whereby" with --in which--; and

in line 13, cancel "now" and cancel "means".

REMARKS

The present Amendment revises the specification and claims to conform to United States patent practice, before examination of the present PCT application in the United States National Examination Phase. All of the changes are editorial and applicant believes no new matter is added thereby. The amendment of claims 1-18 and the addition of claims 19-20 is not intended to be a surrender of any of the subject matter of those claims.

Early examination on the merits is respectfully requested.

Submitted by,

(Reg. No. 45,877)

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APPARATUS AND METHOD FOR THE SYNCHRONIZATION OF AN ASYNCHRONOUS SIGNAL IN SYNTHESIS AND SIMULATION OF A CLOCKED CIRCUIT

The present invention is directed to an apparatus and a method for synchronization of an asynchronous signal in synthesis and simulation of a clocked circuit and, in particular, to an apparatus and a method with which a critical condition can be separated from an uncritical condition in the time behavior of a signal in a clocked circuit in the implementation of a simulation.

Application-specific integrated circuits (ASICs), customer-specific integrated circuit (full-custom ICs) as well as their mixed forms (semi-custom ICs) are being increasingly tested for the logical function and their time behavior in advance by simulation before the manufacture of a corresponding semiconductor component.

A circuit is thereby usually described in a hardware description language such as, for example, a VHDL code, and the logical function of the circuit is tested with a VHDL logic simulator. A test of the time behavior of the signals, however, cannot be implemented with such a logic simulator on the basis of the hardware description language (VHDL code).

For implementing a test of the time behavior of a circuit, on the contrary, the hardware description language (VHDL code) must be converted by a synthesis tool into a network list that represents a further code (circuit plan) for presenting the original circuit. On the basis of this network list, the time behavior of the signals in the circuit can also be acquired or, respectively, tested with a logic/timing simulator.

Given such a test of the time behavior of the signals in the circuit or, respectively, timing simulation, time-critical signal statusses in the circuit can already be recognized and eliminated in the simulation. Let such a signal status be explained by way of example on the basis of a clocked flip-flop, whereby, however, the invention is not limited to such component parts.

Figure a shows a circuit diagram of a traditional flip-flop FF1 with an input terminal D, a clock input CLK and an output terminal Q. Figure 2 shows an exemplary signal-time behavior with which no time-critical signal status occurs in the clocked flip-flop FF1. Characteristics typical of the component derive dependent on the technology respectively employed or, respectively, on the technical realization of an electronic component (for example, flip-flop) in a semiconductor. The characteristics critical for the flip-flop FF1 according to Figure 1 are thereby the setup time t_s and the hold time t_h. These times define a time span for the flip-flop FF1 shown in Figure 1 before and after the leading edge of the clock signal CLK at which a dependable acceptance of a signal pending at the input D ensues. Since, according to Figure 2, the signal at the input D already has a stable value "1" before the time span t_s and t_h, the signal at the output Q of the flip-flop FF1 is dependably set to "1" at the time of the leading edge of the clock signal CLK.

Compared thereto, Figure 3 shows a signal-time behavior with which a violation of the setup time t_s occurs, for which reason the output Q assumes an undefined condition. According to Figure 3, the leading edge of the signal at the input of the flip-flop FF1 falls into the time span t_s of the setup time, for which reason the signal at the output Q initially proceeds into a metastable condition I in order to then assume an undefined but fixed condition II ("0" or "1") after the time t_m. The metastable condition has an approximate time duration $t_m = 5 \times t_{PD}$, whereby t_{PD} is the running time in the flip-flop FF1 from the clock input CLK to the output Q. The time duration for t_m for the metastable condition I is dependent on the technology employed and on the semiconductor employed. After the metastable condition I, wherein the output signal Q usually oscillates, the output signal Q enters into a stable but undefined condition II that is arbitrarily and randomly assumed. The same is true given violation of the hold time.

Such unknown, i.e. metastable or, respectively, undefined conditions in the signal-time behavior are undesired since they disadvantageously influence the

following circuit elements that interpret this signal and are referred to in general below as setup/hold time violations.

Particularly in the implementation of a logic/timing simulation or, respectively, test of the signal-time behavior of a clock circuit, the above-described setup/hold time violation has such an effect that the simulator outputs an "unknown" status for the affected signal, and signals or, respectively, circuit elements that are dependent on this signal in circuit-oriented terms can no longer be tested. This leads to considerable problems in a majority of applications (abort of the simulation).

Figure 4 shows a clock circuit that is composed of a first ASIC module A1 and of a second ASIC module A2. The ASIC module A1 is operated with a first clock signal CLKI, for example 16 MHz, and the ASIC module A2 is operated with a second clock signal CLKII, for example 25 MHz. The clocks CLKI and CLKII are not synchronized, as a result whereof the problems derives that the ASIC module A1 output an output signal S_ASYNC that is asynchronous relative to the clock signal CLKII. The signal A_ASYNC is asynchronous relative to the input clock signal CLKII. Setup/hold time violations can thus necessarily occur in an input circuit of the ASIC module A2. Given a logic/timing simulation of the circuit to be implemented according to Figure 4, the entire ASIC module A2 can thus not be tested in view of its time behavior since there is the potential risk of setup/hold time violations at the input FF of ASIC module A2. In order to avoid such an outcome, the test of a setup/hold time violation can be generally disabled or the signal curve of the respective signals is intentionally modified for the implementation of the simulation; for example, the signal S_ASYNCH is generated synchronous with the clock CLKII. A further possibility is comprised in undertaking a manual intervention into the network list of the circuit to be simulated in order to selectively deactivate the test or, respectively, the setup time violation form the input circuit (flip-flop).

All of these measures, however, are time-consuming, susceptible to error or deteriorate the simulation result since the simulation is not based on the real time behavior of the signals.

The invention is therefore based on the object of creating an apparatus and a method for synchronizing an asynchronous signal in synthesis and simulation of a clocked circuit, whereby the entire circuit can be tested in a simple way with respect to setup/hold time violations.

This object is achieved by the measures indicated in patent claim 1 in view of the method. In view of the apparatus, this object is achieved by the features recited in patent claim 10.

Inventively, thus a circuit is first described with a hardware description language and the existing asynchronous signals are marked. A synthesis of the hardware description subsequently ensues for producing a network list, whereby a synchronization module is inserted at every marking. A logic/timing simulation is implemented with this network list, whereby the testing of the time behavior is deactivated for each inserted synchronization module. All further undefined signal-time behaviors that still occur are indicated.

Thus, clocked circuits having a plurality of signals that are asynchronous relative to one another can be completely tested in view of their time behavior without involved counter-measures for acquiring unavoidable but undefined statusses being thereby required.

For example, an imaginary flip-flop can be inserted as synchronization module, this being composed of two series-connected flip-flops, whereby a setup/hold time violation test for the first flip-flop is automatically deactivated in the implementation of the timing simulation.

The invention is described in greater detail below on the basis of exemplary embodiments with reference to the drawings. Shown are:

Figure 1 a circuit diagram of a clocked flip-flop for illustrating setup/hold time violations;

Figure 2 an illustration of the signal-time curves in the flip-flop according to Figure 1, whereby no unknown statusses occur;

Figure 3 an illustration of the signal-time curves in the flip-flop according to Figure 1, whereby unknown statusses occur;

Figure 4 a block circuit diagram of a clocked circuit with asynchronous signals;

Figure 5 a block circuit diagram of a circuit for illustrating the conversion into a hardware description language;

Figure 6 an illustration of the inventively generated network list for the circuit according to Figure 5;

Figure 7 an illustration of the network list of a further exemplary embodiment for the imaginary flip-flop according to Figure 6;

Figure 8 a block circuit diagram with a logic causing a setup-time violation;

Figure 9 an illustration of the signal-time curves of the circuit according to Figure 6; and

Figure 10 an illustration of the signal-time curves of the circuit according to Figure 8.

Figure 5 shows an illustration of a block circuit diagram for illustrating the functioning of the inventively method. A circuit part A1 thereby corresponds to the ASIC module A1 shown in Figure 4, whereas a circuit part A2 in Figure 5 corresponds to the ASIC module A2 according to Figure 4. The circuit is first described by a hardware description language. A frequently employed hardware description language is thereby the VHDL code, whereby, however, different hardware description languages can also be applied to the present invention. The circuit part A1 comprising [sic] an AND-gate AND and a clocked flip-flop FF1 and is described below in the VHDL code by way of example:

```
process A1 (CLK1)
begin
        wait until (CLKI'event and CLK= "1");
        C <= A & B;
end process;
```

```
process A21 (CLKI)
begin
        wait until (CLKI'event and CLKI= "1");
        S3 <= S2;
end process;

process A22 (CLKII)
begin
        wait until (CLKII'event and CLKII= "1");
        S4 <= S3;
end process;
```

The circuit part A1 and A2 according to Figure 5 is described in view of its logical function with this VHDL code. A logical test of the circuit can be undertaken on the basis of this VHDL code with a VHDL logic simulator.

As already mentioned in the introduction to the specification, however, a timing simulation cannot be implemented on the basis of this VHDL code. On the contrary, a network list that serves as the basis for the logic/timing simulation must be acquired by synthesis from the hardware description language for the time analysis of the circuit according to Figure 5.

A network list that essentially corresponds to the block circuit diagram according to Figure 5 arises in the implementation of a traditional synthesis. As already mentioned in the introduction to the specification, however, setup time violations can thereby occur in the flip-flop FF2, since the flip-flop FF2 is supplied with a signal S2 that is not synchronous or, respectively, is asynchronous relative to the clock signal CLKII. Thus, the metastable or, respectively, undefined statusses shown in Figure 3 can occur at the output Q of the flip-flop FF2 and all of the following circuit regions in the circuit part A2 can no longer be tested.

Figure 6 shows a block circuit diagram of a network list like that generated with the inventive method or, respectively, the inventive apparatus.

First, all circuit components of the circuit according to Figure 5 are described in a hardware description language, whereby all asynchronous signals are marked in a suitable way (for example, ASYNC signal S2...). The VHDL code that has arisen in this way is now checked with a VHDL logic simulator in view of the logical functions of the circuit according to Figure 5. A synthesis of the VHDL code subsequently ensues for producing a network list, whereby a synchronization module or, respectively, an imaginary flip-flop IFF according to Figure 6 is inserted for each correspondingly marked asynchronous signal. This synchronization module serves for the synchronization of the asynchronous signal S2. The remaining elements such as, for example, the AND-gate 'AND' and the flip-flop FF1 remain unmodified in the network list.

Figure 9 shows an illustration of the critical signal-time curves according to Figure 5. CLKI references a clock signal that is input to a flip-flop FF1 at its clock input. A signal S1 that derives from the AND operation of the signals A and B is input at he input terminal D of the flip-flop FF1. The signal S2 shows the output signal of the flip-flop FF1 that is supplied to a flip-flop FF2 at its D-input as asynchronous signal S2 (sync). According to Figure 9, the signal S2 rises to the value "1" at the time t_1 when the leading edge of the clock signal CLKI is adjacent at the flip-flop FF1. Since the input signal S1 is already adjacent in stable form for an adequately long time, no unknown statusses arise. In the same way, an output signal S3 of the flip-flop FF2 is set to the value "1" at time t_2 when the leading edge of a second clock signal CLKII is adjacent. In this case, too, no unknown signal statusses arise for the signal S3, since the input signal of the flip-flop FF2 is already adjacent in stable form for an adequately long time.

Due to the fact, however, that the clock signals CLKI and CLKII are not synchronized with one another and, over and above this, exhibit different clock frequencies, a setup time violation of the flip-flop 2 can occur at time t_3. As shown in Figure 9, namely, the leading edge of the clock signal CLKII that triggers the second flip-flop FF2 can essentially coincide with the trailing edge of the signal S2, so that no

completely defined signal for the flip-flop FF2 is present in the critical time span of the setup time.

As was already described on the basis of Figure 3, such an unstable condition initially produces a metastable condition with the time duration t_m at the input terminal of a flip-flop, the output signal S3 oscillating during this time and then assuming an arbitrary, undefined but fixed status. This status at time t_3 is usually interpreted as unknown status, for which reason an unknown status is likewise allocated to a further consideration of the time behavior of the signals dependent thereon.

According to the inventive method, however, an imaginary flip-flop IFF23 (= synchronization FF) according to Figure 6 is inserted into the network list at a marked, asynchronous signal in a circuit to be simulated. Setup/hold time violations are suppressed for this specific element in a suitable way (for example, with corresponding adaptations in the simulation model of the IFF23), for which reason the output signal of the imaginary flip-flop IFF23 is a defined signal and causes no problems in the logic/timing simulation.

In combination with a modified logic/timing simulation wherein the test of the time behavior for each inserted, imaginary flip-flop IFF (or, respectively, a part of the flip-flop IFF) is deactivated in a suitable way, a complete test of the signal-time behavior in the circuit can thus ensue for a clocked circuit with asynchronous signals. All other undefined statusses to be detected, namely, can be reliably acquired, as follows from Figure 8.

Figure 8 shows a block circuit diagram of a circuit with a faulty dimensioning of the logic DL acting as delay element that, for example, can follow at the output S_{out} of Figure 5. The faulty dimensioning of the logic DL acting as delay element effects a violation of the setup time of the following flip-flop FF_{out}.

Figure 10 shows an illustration of the signal-time curves of the critical signals according to Figure 8, whereby the time t_{logic} represents the delay time of the logic DL. According to Figure 10, setup/hold time violations can likewise occur at

the input of the flip-flop FF_{out} given poor dimensioning of the logic DL. According to Figure 8, an input fli-flop FFin and an output flip-flop FFout are clocked with the same clock signal CLK. An input signal S_{in} is set to "1" with a leading edge of the clock signal CLK and is again set to "0" with the next leading clock edge. This signal S1 is supplied to the logic circuit DL that is supplied [sic] located between the input flip-flop FFin and the output flip-flop FFout. Due to the gate running times of the logic DL, a time delay of the signal arises that can lead to a case as shown in Figure 10 given poor dimensioning of the circuit. According to Figure 10, the leading edge of the signal S2 delayed by the delay time t_{logic} of the logic circuit DL coincides with the leading edge of the clock signal CLK, as a result whereof a setup time violation derives. Due to the lack of an adequately stable input signal at the input terminal D of the output flip-flop FFout, an unknown status, which derives from the aforementioned metastable status and the undefined status, is obtained for an output signal Sout at the output terminal Q of the flip-flop FFout.

Such unwanted statusses can continue to be detected and localized in the logic/timing simulation, wherewith [sic] a synchronization module for a marked asynchronous signal is merely inserted with the inventive method and the test for setup/hold time violation is selectively deactivated.

Figure 7 shows another exemplary embodiment of a flip-flop IFF to be inserted in the network list. The imaginary flip-flop or, respectively, synchronization module is thereby again composed of a flip-flop FF2 and a flip-flop FF3, whereby an inverter INV, however, is additionally inserted that generates the clock signal $\overline{CLK}$ by inverting the clock signal CLK supplied to the flip-flop FF2. As a result thereof, the signal S4 output at the flip-flop 3 is already ready after one clock cycle.

The present invention was described only on the basis of clocked flip-flops that are set with the leading edge. However, flip-flops can also be employed that are set with the trailing edge, or a combination of these two types of flip-flop is employed. Further, the present invention is not limited to clocked flip-flops but, on the contrary, relates to all types of clocked circuit elements wherein the above-

described events for generating unknown statusses can occur. In particular, the employment of two flip-flops for the synchronization module inserted into the network list can be arbitrarily changed, as long as it allows a synchronization of two asynchronous signals with respect to its time behavior and -- over and above this -- a setup time violation can be designationally deactivated.

Figure 11 shows a flowchart of the above-described inventive method. In a step S1, first, an arbitrary circuit for which an ASIC, a full-custom IC or a semi-custom IC is to be fabricated is described with a hardware description language. All asynchronous signals or signal lines are thereby already marked. In the step S2, for example, a logic simulation of the VHDL code produced in this way can be implemented, whereby the purely logical operations of the circuit are tested. A synthesis of the hardware description language or, respectively, of the VHDL code for producing a network list follows in step S3, whereby a pre-defined synchronization module is inserted into the network list at the marked signals. A specific timing simulation is implemented in step S4 on the basis of this modified network list of the initial circuit, whereby the test of setup/hold time violations is selectively deactivated for each inserted synchronization module or at least a part of this synchronization module. All undefined signal-time behaviors still occurring in the synchronous signal paths, i.e. unknown statusses following setup/hold time violations, continue to be detected and displayed. A VHDL code is preferably employed as hardware description language in the present invention. However, all other hardware description languages can be employed in the same way insofar as they allow a marking of asynchronous signals or, respectively, signal lines. Likewise, all types of synthesis tools can be employed with which a network list can be produced from a hardware description language and the insertion of a synchronization module is possible given occurrence of a marking. In the same way, all types of simulators can be employed for the timing simulations with which the inserted synchronization module or at least a part of this module can be selectively deactivated in view of the testing of the time behavior.

Figure 12 shows an apparatus for the implementation of the above-described method. The apparatus is essentially composed of an input means 1, of a first memory means 2 for storing the hardware description language (VHDL code) and of a second memory 3 for storing the second code produced in the synthesis, i.e. the network list. A marking means 4 selectively marks all asynchronous signals or, respectively, signal lines found in the hardware description language, whereas a logic simulator 8 implements a logic simulation for testing the logic functions of the circuit on the basis of the hardware description language. A synthesis means 6 implements a synthesis of the hardware description language (VHDL code) that is marked and deposited in the memory 2, as a result whereof a modified network list arises that is deposited in the memory 3. As was already set forth above, the network list deposited in the memory 3 has the inserted synchronization modules. A logic/timing simulator 7 implements a logic/timing simulation at the network list stored in the memory 3, whereby it is configured such that no test of setup/hold time violations is implemented in the synchronization module or parts of this module. The results acquired by the logic simulator and timing simulator are output via a display means 5, whereby the circuit element causing the time infraction is optionally co-displayed. The means 1 through 8 are preferably connected to one another via a bus structure 9, whereby the synthesis means 6, the timing simulator 7 and the logic simulator can be realized by one or more CPUs (central units) with appertaining memory units (ROMs).

Patent Claims

1. Method for the synchronization of an asynchronous signal in synthesis and simulation of a clocked circuit

a) describing the clocked circuit with a first code (VHDL) in a hardware description language;

b) marking asynchronous signals of the clocked circuit in the first code (VHDL);

c) implementing a synthesis of the first code (VHDL) for producing a second code in a network list format, whereby a synchronization module (IFF) is inserted at every marking;

d) implementing a logic/timing simulation at the second code for testing the time behavior of the signals in the clocked circuit, whereby the test of the time behavior is selectively deactivated for each inserted synchronization module (IFF) by adaptation in the simulation model of the appertaining synchronization module; and

e) displaying occurring, undefined signal-time behavior in the clocked circuit.

2. Method according to patent claim 1, comprising the further step: implementing a logic simulation at the first code (VHDL) for testing the logic function of the clocked circuit.

3. Method according to patent claim 1 or 2, whereby the first code represents a hardware description language and the second code represents a network list.

4. Method according to patent claim 3, whereby the hardware description language as a VHDL code.

5. Method according to one of the claims 1 through 4, whereby the insertion of the synchronization module implemented in the synthesis of the first code corresponds to the insertion of an imaginary flip-flop (IFF).

6. Method according to patent claim 5, whereby the imaginary flip-flop (IFF) is composed of a first and second flip-flop (FF2, FF3) that are clocked with the same clock.

7. Method according to patent claim 5, whereby the imaginary flip-flop (IFF) is composed of a first and a second flip-flop (FF2, FF3) that are clocked with clocks (CLK, $\overline{CLK}$) inverted relative to one another.

8. Method according to one of the patent claims 6 or 7, whereby the test of the signal-time behavior upon implementation of the timing simulation is selectively deactivated only for the first flip-flop (FF2).

9. Method according to one of the patent claims 1 through 8, whereby a circuit element causing an undefined signal-time behavior is displayed when the undefined signal-time behavior is displayed.

10. Apparatus for detecting undefined signal-time behavior in a clocked circuit comprising

a) an input means (1) for the input of a first code (VHDL) describing a clocked circuit in a hardware description language;

b) a first memory means (2) for storing the first code (VHDL);

c) a marking means (4) for marking asynchronous signals (S_ASYNC) in the first code;

d) a synthesis means (6) that produces a second code in a network list format from the first code (VHDL) and stores this in a second memory means (3), whereby a synchronization module (IFF) is inserted at every marking;

e) a timing simulator (7) that implements a timing simulation at the second code for testing the time behavior of the signals of the clocked circuit, whereby the test of the time behavior is selectively deactivated for each inserted synchronization module (IFF) by adaptation in the simulation model of the appertaining synchronization module;

f) a display means (5) for displaying occurring, undefined signal-time behavior; and

g) a bus structure that connects the means (1-7) to one another.

11. Apparatus according to patent claim 10 with a logic simulator (8) that implements a logic simulation on the basis of the first code (VHDL) for testing the logic behavior of the clocked circuit.

12. Apparatus according to one of the patent claims 10 or 11, whereby the first codes represents a hardware description language and the second code represents a network list.

13. Apparatus according to patent claim 12, whereby the hardware description language is a VHDL code.

14. Apparatus according to one of the patent claims 10 through 13, whereby the synchronization module corresponds to an imaginary flip-flop (IFF).

15. Apparatus according to patent claim 14, whereby the imaginary flip-flop (IFF) is composed of a first and second flip-flop (FF2, FF3) that are clocked with a same clock signal (CLK).

16. Apparatus according to patent claim 14, whereby the imaginary flip-flop (IFF) is composed of a first and a second flip-flop (FF2, FF3) that are clocked with clock signals (CLK, $\overline{CLK}$) inverted relative to one another.

17. Apparatus according to one of the patent claims 15 or 16, whereby the timing simulator (7) does not consider the time behavior for the first flip-flop (FF2) in the implementation of the timing simulation.

18. Apparatus according to one of the patent claims 1 through 17, whereby the display means (5) also displays a circuit element causing the undefined signal-time behavior.

Abstract

Apparatus and Method for the Synchronization of an Asynchronous Signal in Synthesis and Simulation of a Clocked Circuit

An apparatus and a method for the synchronization of an asynchronous signal in synthesis and simulation of a clocked circuit are disclosed, whereby a circuit to be simulated and tested is described with a hardware description language and the asynchronous signals present therein are marked. For producing a network list, the hardware description language is processed with a synthesis tool, whereby a specific synchronization module is inserted at every marking. For testing the time behavior of the signals in the clocked circuit on the basis of the network list, a simulator implements a logic/timing simulation, whereby a test of the time behavior is selectively deactivated for each inserted synchronization module. The unknown statusses that now still occur are output via a display means.

FIG 1

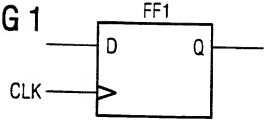


FIG 2

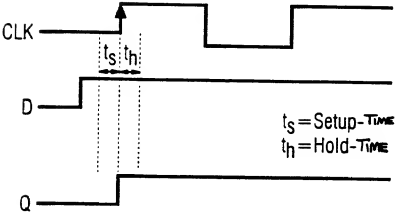


FIG 3

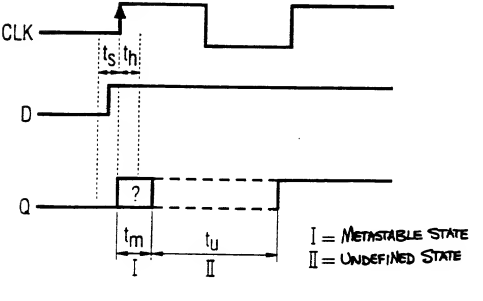


FIG 4

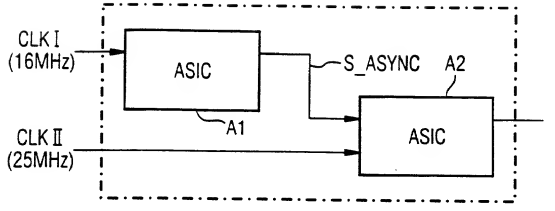


FIG 5

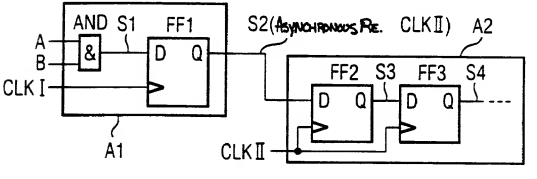


FIG 6

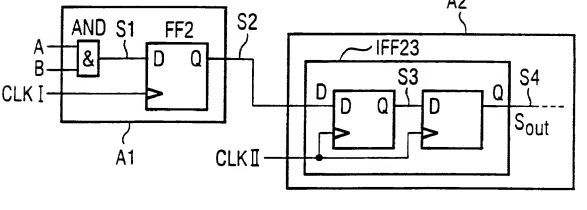


FIG 7

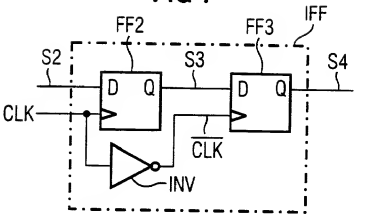

FF2
FF3
IFF
S2
S3
S4
D
Q
D
Q
CLK
CLK
INV

FIG 8

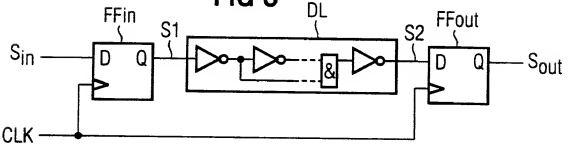

FFin
S1
DL
S2
FFout
Sin
D
Q
&
D
Q
Sout
CLK

FIG 9

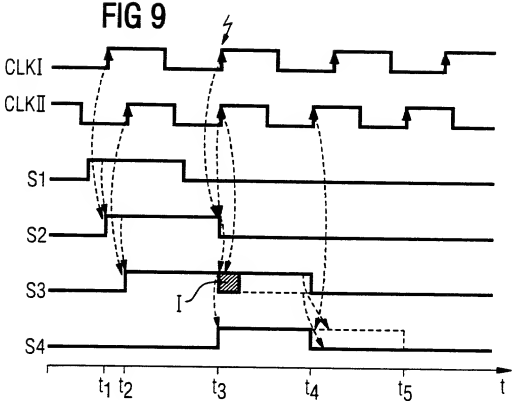


FIG 10

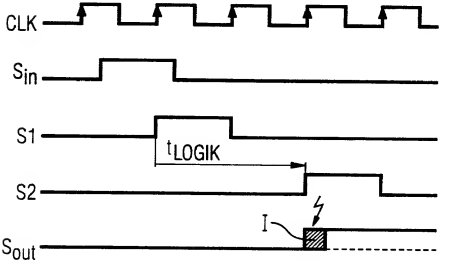


FIG 11

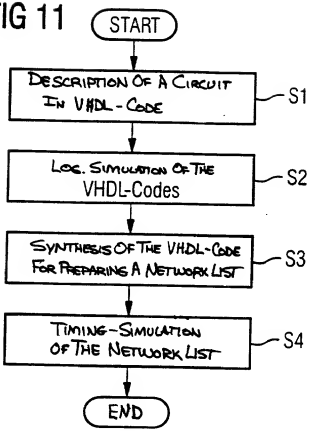
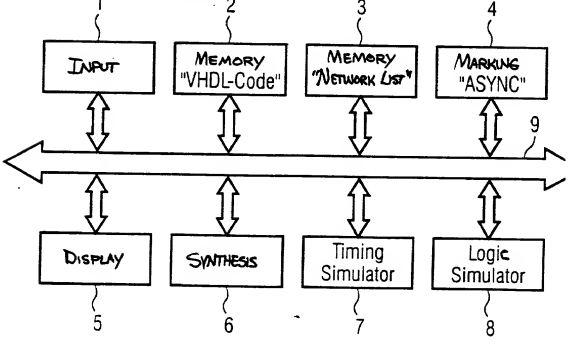

START
DESCRIPTION OF A CIRCUIT IN VHDL-CODE
S1
LOG. SIMULATION OF THE VHDL-Codes
S2
SYNTHESIS OF THE VHDL-CODE FOR PREPARING A NETWORK LIST
S3
TIMING-SIMULATION OF THE NETWORK LIST
S4
END

FIG 12


1
2
3
4
INPUT
MEMORY "VHDL-Code"
MEMORY "NETWORK LIST"
MARKING "ASYNC"
9
DISPLAY
SYNTHESIS
Timing Simulator
Logic Simulator
5
6
7
8

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

My residence, post office address and citizenship are as stated below next to my name,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Vorrichtung und Verfahren zur Synchronisation eines asynchronen Signals in Synthese und Simulation einer getakteten Schaltung

deren Beschreibung

the specification of which

(zutreffendes ankreuzen)

(check one)

☒ hier beigefügt ist.

☒ is attached hereto.

☐ am _____ als PCT internationale Anmeldung PCT Anmeldungsnummer _____ eingereicht wurde und am _____ abgeändert wurde (falls tatsachlich abgeändert).

☐ was filed on _____ as PCT international application PCT Application No. _____ and was amended on _____ (if applicable)

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign appplications
Priorität beansprucht

			Priority Claimed	
198 24 151.8	Germany	29. Mai 1998	☒	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
			☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
			☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsatzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent- und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

And I hereby appoint

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